CLAIMS

What is claimed is:

1. A method of forming chip-scale packages, comprising;

providing a semiconductor wafer having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material;

cutting at least one channel in the active surface of the semiconductor wafer along the at least one street of semiconductor material to expose a plurality of semiconductor die side surfaces;

etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects;

forming a first protective coating on the semiconductor wafer to cover the active surface and fill the at least one channel; and

separating the semiconductor wafer along the at least one channel to form a plurality of individual chip-scale packages.

2. The method of claim 1, wherein cutting at least one channel in the active surface of the semiconductor wafer comprises cutting the at least one channel with one of a dicing saw and a laser beam.

3. The method of claim 1, wherein forming the first protective coating on the semiconductor wafer comprises:

applying a liquid polymer material over the active surface of the semiconductor wafer; and

at least partially curing the liquid polymer material.

4. The method of claim 3, wherein applying the liquid polymer material comprises one of spraying or spin coating the liquid polymer material onto the active surface of the semiconductor wafer.

5. The method of claim 4, wherein each semiconductor die location of the plurality includes at least one bond pad, and further comprising:

etching a portion of the first protective coating to expose the at least one bond pad of each semiconductor die location.

6. The method of claim 3, wherein the liquid polymer material comprises a photocurable liquid polymer material, and further comprising:

exposing the photocurable liquid polymer material to a source of electromagnetic radiation to at least partially cure a portion of the photocurable liquid polymer material.

7. The method of claim 6, wherein each semiconductor die location of the plurality includes at least one bond pad, and further comprising:

selectively curing the photocurable liquid polymer material to leave the at least one bond pad of each semiconductor die location exposed through the first protective coating.

8. The method of claim 1, wherein each semiconductor die location of the plurality includes at least one bond pad, and further comprising:

forming a conductive bump on the at least one bond pad of each semiconductor die location.

9. The method of claim 8, wherein forming the conductive bump on the at least one bond pad comprises forming the conductive bump prior to forming the first protective coating on the semiconductor wafer.

10. The method of claim 9, wherein forming the first protective coating comprises:

spraying or spin coating a liquid polymer material onto the active surface of the semiconductor wafer; and

at least partially curing the liquid polymer material.

11. The method of claim 10, further comprising:

etching a portion of the first protective coating to expose the conductive bump on the at least one bond pad of each semiconductor die location.

12. The method of claim 9, wherein forming the first protective coating comprises:

applying a photocurable liquid polymer material over the active surface of the semiconductor wafer; and

exposing the photocurable liquid polymer material to a source of electromagnetic radiation to at least partially cure a portion of the photocurable liquid polymer material.

13. The method of claim 12, further comprising:

selectively curing the photocurable liquid polymer material to leave the conductive bump on the at least one bond pad of each semiconductor die location exposed through the first protective coating.

14. The method of claim 1, wherein the semiconductor wafer has a passive surface opposite the active surface, and further comprising:

removing a layer of semiconductor material from the passive surface of the semiconductor wafer to a depth sufficient to expose the first protective coating within the at least one channel; and

forming a second protective coating on the semiconductor wafer to cover the passive surface.

15. The method of claim 14, wherein removing the layer of semiconductor material comprises planarizing the passive surface of the semiconductor wafer with at least one of a mechanical process and a chemical process.

16. The method of claim 15, wherein removing the layer of semiconductor material comprises backgrinding the passive surface of the semiconductor wafer.

17. The method of claim 15, wherein removing the layer of semiconductor material comprises a CMP process.

18. The method of claim 14, further comprising:

etching the passive surface of the semiconductor wafer such that the first protective coating exposed within the at least one channel forms at least one frame element protruding from the passive surface of the semiconductor wafer; and

anchoring the second protective coating to the passive surface of the semiconductor wafer with the at least one frame element.

19. The method of claim 1, wherein each semiconductor die location of the plurality of semiconductor die locations comprises a plurality of circuit layers extending a depth into the semiconductor wafer from the active surface of the semiconductor wafer, and wherein cutting at least one channel in the active surface of the semiconductor wafer comprises cutting the at least one channel to a depth that is greater than the depth of the circuit layers within the semiconductor wafer.

20. The method of claim 1, wherein etching the plurality of semiconductor die side surfaces comprises etching the plurality of semiconductor die side surfaces with an anisotropic etching process.

21. A method of forming chip-scale packages, comprising;

providing a semiconductor wafer having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material;

forming a first protective coating on the semiconductor wafer to cover the active surface;

cutting at least one channel in a passive surface of the semiconductor wafer along the at least one street of semiconductor material to expose a plurality of semiconductor die side surfaces;

etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects and to expose the first protective coating within the at least one channel;

forming a second protective coating on the semiconductor wafer to cover the passive surface and fill the at least one channel; and

separating the semiconductor wafer along the at least one channel to form a plurality of individual chip-scale packages.

22. The method of claim 21, wherein cutting at least one channel in the passive surface of the semiconductor wafer comprises cutting the at least one channel with one of a dicing saw and a laser beam.

23. The method of claim 21, wherein forming the first protective coating on the semiconductor wafer comprises:

applying a liquid polymer material over the active surface of the semiconductor wafer; and

at least partially curing the liquid polymer material.

24. The method of claim 23, wherein applying the liquid polymer material comprises one of spraying or spin coating the liquid polymer material onto the active surface of the semiconductor wafer.

25. The method of claim 24, wherein each semiconductor die location of the plurality includes at least one bond pad, and further comprising:

etching a portion of the first protective coating to expose the at least one bond pad of each semiconductor die location.

26. The method of claim 23, wherein the liquid polymer material comprises a photocurable liquid polymer material, and further comprising:

exposing the photocurable liquid polymer material to a source of electromagnetic radiation to at least partially cure a portion of the photocurable liquid polymer material.

27. The method of claim 26, wherein each semiconductor die location of the plurality includes at least one bond pad, and further comprising:

selectively curing the photocurable liquid polymer material to leave the at least one bond pad of each semiconductor die location exposed through the first protective coating.

28. The method of claim 21, wherein each semiconductor die location of the plurality includes at least one bond pad, and further comprising:

forming a conductive bump on the at least one bond pad.

29. The method of claim 28, wherein forming the conductive bump on the at least one bond pad comprises forming the conductive bump prior to forming the first protective coating on the semiconductor wafer.

30. The method of claim 29, wherein forming the first protective coating comprises:

spraying or spin coating a liquid polymer material onto the active surface of the semiconductor wafer; and

at least partially curing the liquid polymer material.

31. The method of claim 30, further comprising:

etching a portion of the first protective coating to expose the conductive bump on the at least one bond pad of each semiconductor die location.

32. The method of claim 29, wherein forming the first protective coating comprises:

applying a photocurable liquid polymer material over the active surface of the semiconductor wafer; and

exposing the photocurable liquid polymer material to a source of electromagnetic radiation to at least partially cure a portion of the photocurable liquid polymer material.

33. The method of claim 32, further comprising:

selectively curing the photocurable liquid polymer material to leave the conductive bump on the at least one bond pad of each semiconductor die location exposed through the first protective coating.

34. The method of claim 21, further comprising:

removing a layer of semiconductor material from the passive surface of the semiconductor wafer prior to forming the second protective coating on the semiconductor wafer.

35. The method of claim 34, wherein removing the layer of semiconductor material comprises planarizing the passive surface of the semiconductor wafer with at least one of a mechanical process and a chemical process.

36. The method of claim 35, wherein removing the layer of semiconductor material comprises backgrinding the passive surface of the semiconductor wafer.

37. The method of claim 35, wherein removing the layer of semiconductor material comprises a CMP process.

38. The method of claim 35, wherein removing the layer of semiconductor material comprises etching the passive surface of the semiconductor wafer concurrently with etching the plurality of semiconductor die side surfaces.

39. The method of claim 21, wherein etching the plurality of semiconductor die side surfaces comprises etching the plurality of semiconductor die side surfaces with an anisotropic etching process.

40. A chip-scale package, comprising:

a semiconductor die having an active surface, an opposing passive surface, and a plurality of etched side surfaces extending from the active surface to the passive surface;

a first protective coating extending over the active surface of the semiconductor die; and

a second protective coating extending over the passive surface of the semiconductor die wherein one of the first protective coating and the second protective coating extends over the plurality of etched side surfaces of the semiconductor die.

41. The chip-scale package of claim 40, wherein the first protective coating extends over the plurality of etched side surfaces of the semiconductor die.

42. The chip-scale package of claim 41, wherein a portion of the first protective coating protrudes beyond the passive surface of the semiconductor die and a portion of the second protective coating is adhered to a side of the portion of the first protective coating protruding beyond the passive surface of the semiconductor die.

43. The chip-scale package of claim 40, wherein the second protective coating extends over the plurality of etched side surfaces of the semiconductor die.

44. The chip-scale package of claim 40, wherein at least one of the first protective coating and the second protective coating comprises a polymer sealant material.

45. The chip-scale package of claim 44, wherein the polymer sealant material comprises a photocurable polymer sealant material.